REMARKS

The following is intended as a full and complete response to the Office Action dated January 5, 2010, having a shortened statutory period for response set to expire on April 5, 2010. The Examiner rejected claims 1-5, 7, 10-14, 16, 20-21, 25 and 31-35 under 35 U.S.C. § 103(a) as being unpatentable over Gulick (U.S. Patent No. 5,692,211) in view of Bishop (SPARTA: Simulation of Physics on a Real-Time Architecture) and Dixon (U.S. Patent No. 6,754,732). The Examiner rejected claims 15 and 17 under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Bishop, Dixon and Humphrey (U.S. Patent No. 4,933,846). The Examiner rejected claims 22-24, 29-30 and 36-37 under under 35 U.S.C. §103(a) as being unpatentable over Gulick in view of Bishop, Dixon and Mohamed (U.S. Patent No. 6,366,998). The Examiner rejected claims 26-28 under 35 U.S.C §103(a) as being unpatentable over Gulick in view of Bishop, Dixon and Telekinesys (Havok Game Dynamics SDK). The Examiner rejected claims 38-40 under 35 U.S.C §103(a) as being unpatentable over Gulick in view of Bishop, Dixon and Hirahara (U.S. Patent No. 5,063,498).

Rejections under 35 U.S.C. §103(a)

Amended claim 1 recites the limitations of a floating point engine (FPE) that includes a vector processor configured to perform multiple, parallel floating point operations to generate physics simulation data associated with physics simulation requests, where each parallel floating point operation is specified by a very long instruction word (VLIW) that is issued to the FPE by a PPU control engine (PCE). None of the cited references teaches or suggests these limitations.

Gulick discloses a dedicated multimedia engine that executes commands received from a central processing unit to perform real-time operations, including audio and video operations. The multimedia engine includes a digital signal processing (DSP) engine and dedicated multimedia memory that is coupled directly to a main memory. The DSP engine performs video and audio processing functions on data stored within the multimedia memory and stores microcode corresponding to video and audio processing instructions (see Gulick at column 7, lines 26-30). In the Office Action, the Examiner equates the DSP engine disclosed in Gulick to the claimed FPE. However, Gulick does not disclose or otherwise suggest that the DSP engine performs multiple

audio/video operations in parallel. As described, the DSP engine in Gulick performs audio/video operations serially and does not have any parallel processing capability (see Gulick at column 7, lines 34-41). By contrast, claim 1, as amended, expressly recites that the vector processor within the FPE is configured to perform multiple, parallel floating point operations to generate the physics simulation data.

Further, there is no specific disclosure in Gulick regarding the types of instruction formats that the disclosed DSP engine is configured to execute. More specifically, Gulick does not teach or suggest that the DSP engine processes instructions received from the multimedia processing engine or the CPU that are specified by a very long instruction word (VLIW). Amended claim 1, however, now explicitly recites that the FPE is configured to perform a parallel floating point operation that is specified by a VLIW.

Bishop discloses an application-specific integrated circuit that can accelerate physics modeling in conjunction with a CPU. The Examiner relies on Bishop only to demonstrate a Physics Processing Unit (PPU). Thus, Bishop fails to cure the deficiencies of Gulick set forth above.

The remaining references, Dixon, Humphrey, Mohamed, Telekinesys and Hirahara, also fail to cure the deficiencies of Gulick set forth above.

As the foregoing illustrates, no combination of the cited references can teach or suggest each and every limitation of amended claim 1. Therefore, these references cannot render obvious claim 1 or claims 2-5, 7, 10-17, 20-23 and 38, dependent thereon. For this reason, Applicants submit that claims 1 and claim 2-5, 7, 10-17, 20-23 and 38 are in condition for allowance.

Claims 25 and 31 recite limitations similar to those recited in claim 1 and are, therefore, allowable for at least the same reasons as allowable claim 1. The remaining claims depend from either allowable claim 25 or 31 and, therefore, are also in condition for allowance.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Office Action mailed January 5, 2010 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

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